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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,117	12/17/2001	Bernardo De Oliveira Kastrup Pereira	NL 000721	2411

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,117	DE OLIVEIRA KASTRUP PEREIR ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 17 December 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5, 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-6 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

3. The drawings are objected to because:

3.1. The structural elements are merely labeled with identifying numbers, see Figures 1-3. Since these elements are not illustrated as well known graphical representations, Applicant is required to provide suitable meaningful legends under 37 CFR § 1.83(a) and 1.84(o). Correction is required.

4. Claim 4 is rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4.1. The scope of meaning of the following terms are unclear:

4.1.1. "to the an input or output" claim 4; This construct is not grammatically correct, and it appears that one of the words "the" and "an" is superfluous.

5. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6 are rejected under 35 USC § 102(b) as being clearly anticipated by Hauck et al., *The Chimaera Reconfigurable Functional Unit*, The 5th Annual IEEE Symposium on FPGAs for Custom Computing Machines, April 16-18, 1997.

Hauck et al. taught the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

6.1. A data processing device (fig. 1) that is capable of executing a program comprising an instruction (pg. 88, col. 1, lines 25-32), the device comprising a configurable functional unit (fig. 1, "Reconfigurable Array) for executing the instruction according to a configurable function that is configured outside the instruction (pg. 88, col. 2, lines 14-

17), the configurable functional unit having;

6.2. a unit input (fig. 2, I1 ... I4) and a unit output (O1 ... O4) for inputting and outputting bits of an operand and a result (pg. 89, col. 2, lines 20-21) to a source and destination register specified by the instruction respectively (pg. 88, col. 2, lines 10-17), the configurable functional unit comprising;

6.3. a plurality of independent configurable logic blocks for performing programmable logic operations to implement the configurable function (fig. 2, 4-LUT/2x3-LUT);

6.4. a first programmable connection circuit between the unit input and the logic blocks (fig. 3, 1 .. 4), for selectively coupling inputs of the logic blocks to bits from the unit input, dependent on the configured function (pg. 90, col. 1, lines 4-11);

6.5. a second programmable connection circuit between the logic blocks and the unit output (fig. 3, 6 ... 9, fig. 2, multiplexers connected to O1 ... O4), for selectively coupling bits of the unit output to outputs of the logic blocks, dependent on the configured function (fig. 2, fig. 3).

7. As to claims 2 and 3, Hauck et al. taught that each logic block had a plurality of outputs (fig. 3, F1, F2), at least one of the bits of the unit output being connectable exclusively to one of the outputs of each logic block (fig. 3, 6 ... 9, fig. 2, muxes connected to O1 ... O4), the second programmable connection circuit comprising a multiplexer (fig. 3, 6 ... 9, fig. 2, muxes connected to O1 ... O4) for coupling the one of the outputs of a selected one of the logic blocks to the at least one of the bits of the unit output (fig. 3, muxes 6 ... 9 connect LUT outputs to muxes of fig. 2, fig. 2, muxes connect output of units to unit output O1 ... O4).

8. As to claim 4, Hauck et al. taught that the first programmable connection circuit or the second programmable connection circuit had a fixed unprogrammable connection to the an [sic] input or output of one of the independent configurable logic blocks and a programmable connection to a remainder of the inputs and outputs (fig. 2, I1 and I4 are fixedly copied to O1 ... O4 muxes, while I2, I3, and F1, F2 are selectively connectable to O1 ... O4 muxes).

9. As to claim 5, Hauck et al. taught a method of programming a configurable processing device to perform a processing task (pg. 92, "Application Examples"), wherein the device has a configurable functional unit (fig. 1, "Reconfigurable Array) that comprises several programmable logic blocks (fig. 2), the method comprising:

9.1. identifying a special complex of operations that occurs in the task and requires an operand data word and produces a result data word (pg. 93, col. 1, lines 3-5);

9.2. searching for an assignment of the logic operations for producing different bits of the result to different ones of the programmable logic blocks (fig. 6), so that the logic operations for producing a subset of the bits of the result that, if implemented together in one of the programmable logic blocks, would exceed the capacity of that one of the programmable logic blocks, are distributed over different ones of the logic blocks (fig. 6, instruction one requires two rows, instructions 2 and 3 occupy four rows);

9.3. programming each of the programmable logic blocks to perform the logic operations for the bits of the result assigned to it (fig. 6, "Computation" column);

9.4. programming connection circuits in front of the programmable logic blocks and subsequent to programmable logic blocks so as to route bits of an operand of a special instruction to the programmable logic blocks that use those bits of the operand in the logic operations and so as to route outputs of the programmable logic blocks to bits of the result to which the programmable logic blocks are assigned (pg. 93, col. 2, line 1 to pg. 93, col. 1, line 15).

10. As to claim 6, Hauck et al. taught a method of executing a program with a processing device (fig. 1) with a configurable functional unit (fig. 1, "Reconfigurable Array"), the method comprising the following steps in response to a configuration instruction;

10.1. inputting bits of an operand of the configurable instruction into the configurable function unit (pg. 88, col. 2, lines 38-41);

10.2. selectively coupling the bits of the operands to inputs of logic blocks, dependent on a configured function (pg. 88, col. 2, lines 5-11);

10.3. performing programmable logic operations to implement the configurable function (pg. 88, col. 1, lines 33-36);

10.4. selectively coupling outputs of the logic blocks to bits of a result, dependent on a configured function (pg. 88, col. 1, lines 33-36, pg. 89, col. 2, line 17).

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hutchings et al. disclosed details related to performing the analysis necessary for deriving configurations for reconfigurable funcitonal units.

Sawase et al. disclosed a processor with an attached reconfigurable functional unit.

Razdan et al. disclosed an implimentation of a processor with attached reconfigurable functional units.

Potash et al. disclosed a computing system with both reconfigurable control and reconfigurable functional unit sections.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
September 13, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER